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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/646,218 | 08/22/2003 | Manfred Engelhardt | GR 98 P 2661 D | 1417 |

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LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

| EXAMINER | |
|---|---|
| NGUYEN, DILINH P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/646,218 | ENGELHARDT, MANFRED | |
| | Examiner | Art Unit | |
| | DiLinh Nguyen | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Mori et al. (U.S. Pat. 6335570) (newly cited).

Mori et al. disclose a method of producing an integrated circuit configuration, with comprises:

forming a diffusion barrier layer 6 on a substrate 1 having at least a first insulating layer 2 with a first conductive structure 5 embedded therein, the diffusion barrier layer covering the first conductive structure completely (fig. 16);

forming a second insulating layer 7 on the diffusion barrier layer;

etching a contact hole 8 into the second insulating layer above the first conductive structure 5 without uncovering the first conductive structure 5, and with a surface of the first conductive structure being covered with the diffusion barrier layer within the hole (fig. 16);

forming spacers 31 on side walls of the contact hole, the spacers acting as a barrier to diffusion of a material from the first conductive structure into the second insulating layer (fig. 16);

subsequently opening the contact hole as far as a surface of the first conductive structure (fig. 17); and

forming in the contact hole a second conductive structure 10 conductively connected to the first conductive structure (fig. 18).

- Regarding claim 2, Mori et al. disclose forming the spacers 31 of electrically conductive material (fig. 17, column 11, lines 4-5).
- Regarding claim 3, Mori et al. disclose forming the first electrically conductive structure 5 by applying the first insulating layer 2 to the substrate 1; producing an opening with a bottom and side walls in the first insulating layer; depositing and structuring a first conductive barrier layer for forming an electrically conductive first diffusion barrier structure 4 covering the bottom and the side walls of the opening; and forming the first conductive structure 5 by filling the opening with conductive material (figs. 2-3).
- Regarding claims 4 and 6, Mori et al. disclose depositing a second conductive barrier layer 42 after the contact hole has been opened as far as the surface of the first conductive structure;

  depositing a conductive structure 10;

  structuring the conductive layer and the second conductive barrier layer, and thereby forming the second conductive structure 10 and a second diffusion barrier structure 42 arranged underneath the second conductive structure 10 (fig. 18).

- Regarding claim 5, Mori et al. disclose forming one of the first conductive structure 5 and the second conductive structure 10 with a material selected from the group consisting of copper (fig. 18, column 6, lines 44);

  forming one of the spacers 41, the first diffusion barrier structure 4 and a second diffusion barrier structure 42 with Ta (fig. 18, column 11, lines 4-5);

  forming one of the diffusion barrier layer 6 with a material selected from the group consisting of SiN (fig. 18, column 6, lines 22-23).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. (U.S. Pat. 6100184) (newly cited) in view of Mori et al. (U.S. Pat. 6335570) (newly cited).

Zhao et al. disclose a method of producing an integrated circuit configuration, which comprises:

forming a diffusion barrier layer 13 on a substrate having at least a first insulating layer 11 with a first conductive structure 10 embedded therein, the diffusion barrier layer covering the first conductive structure completely (fig. 8);

forming a second insulating layer 14 on the diffusion barrier layer;

etching a contact hole 24 into the second insulating layer above the first conductive structure 10 without uncovering the first conductive structure, and with a surface of the first conductive structure being covered with the diffusion barrier layer within the hole (fig. 10);

forming spacers 28 on side walls of the contact hole, the spacers acting as a barrier to diffusion of a material from the first conductive structure into the second insulating layer (fig. 12, column 8, lines 20-25);

opening the contact hole as far as a surface of the first conductive structure; and

forming in the contact hole a second conductive structure 29 conductively connected to the first conductive structure (fig. 12).

Zhao et al. fail to disclose the step of subsequently opening the contact hole as far as a surface of the first conductive structure.

However, Mori et al. disclose a method of producing an integrated circuit configuration, which comprises: etching a contact hole 8 into the second insulating layer 7 above the first conductive structure 5 without uncovering the first conductive structure; forming spacers 9 on side walls of the contact hole; subsequently opening the contact hole as far as a surface of the first conductive structure (fig. 7). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Zhao et al. by having the step of subsequently opening the contact hole as far as a surface of the first conductive structure, as taught by Mori et al., in order to protect the expose surface of the conductive structure (fig. 6).

- Regarding claim 2, Zhao et al. disclose forming the spacers 28 of electrically conductive material (fig. 12, column 8, lines 20-23).
- Regarding claim 3, Zhao et al. disclose forming the first electrically conductive structure 10 by applying the first insulating layer to the substrate 11; producing an opening with a bottom and side walls in the first insulating layer; depositing and structuring a first conductive barrier layer for forming an electrically conductive first diffusion barrier structure 12 covering the bottom and the side walls of the opening; and forming the first conductive structure 10 by filling the opening with conductive material (fig. 13).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al. (U.S. Pat. 6100184) (newly cited) in view of Jain (U.S. Pat. 5821168) (newly cited).

Zhao et al. disclose a method of producing an integrated circuit configuration, which comprises:

forming a diffusion barrier layer 13 on a substrate having at least a first insulating layer 11 with a first conductive structure 10 embedded therein, the diffusion barrier layer covering the first conductive structure completely (fig. 8);

forming a second insulating layer 14 on the diffusion barrier layer;

etching a contact hole 24 into the second insulating layer above the first conductive structure 10 without uncovering the first conductive structure, and with a surface of the first conductive structure being covered with the diffusion barrier layer within the hole (fig. 10);

opening the contact hole as far as a surface of the first conductive structure; and

forming in the contact hole a second conductive structure 29 conductively connected to the first conductive structure and a second diffusion barrier structure 28 arranged underneath the second conductive structure (fig. 12).

Zhao et al. fail to disclose a step of forming layers on side walls of the contact hole, the layers acting as a barrier to diffusion of a material from the first conductive structure into the second insulating layer.

However, Jain discloses a method of producing an integrated circuit configuration, which comprises: forming spacers 56 on side walls of the contact hole, the spacers acting as a barrier to diffusion of a material from the first conductive structure 28 into the second insulating layer 26 (fig. 6, column 4, lines 58-59). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Zhao et al. by forming the diffusion barrier spacers on side walls of the contact hole, as taught by Jain, in order to decrease the resistance for the integrated circuit device (column 5, lines 50-52).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

HOAI PHAM
PRIMARY EXAMINER